REMARKS

Claims 1-11 are pending in the application.

By this Amendment, claims 1 and 11 have been amended to more particularly point out and distinctly claim the invention. No new matter has been added. Applicants expressly reserve the right to pursue broader claims and/or to appeal any or all rejections.

35 U.S.C. § 103(a) Rejection

Claims 1-11 presently stand rejected under 35 U.S.C. § 103(a) over Hino, et al (U.S. Patent No. 5,117,468) in view of Horiguchi (U.S. Patent No. 4,680,643). Because the proposed combination of Hino and Horiguchi does not disclose or suggest all of the limitations of claims 1-11, it is asserted that claims 1-11 are patentable over the cited art.

Specifically, with respect to claim 1 (and claims 2-5, which depend from claim 1), this claim as amended recites "a plurality of processors processing respective input image data in parallel with each other ...and an address memory storing address information for each respective image data while being processed by said plurality of processors."

This limitation is not disclosed or suggested by the proposed combination of Hino and Horiguchi. Hino discloses an image processing system comprising cascaded shift registers and one or more image processing circuits. However, as noted in the Office Action, Hino fails to disclose an address memory for storing address information as recited in claim 1. It is respectfully asserted that, contrary to the allegation in the Office Action, Horiguchi fails to cure this deficiency of Hino with respect to the present rejection.

Horiguchi is directed towards a system for displaying multiple images on a screen, such as a CRT display. Horiguchi discloses an image display apparatus for controlling the display of the multiple images that includes an address register for each image to be displayed. Image data from the multiple images is stored in a video RAM. A video RAM

address for the data is generated by an adder based on which address register the data is referenced from, offset by an output from counters that track current line and column of the display plane. However, Horiguchi is not concerned with image processing. Instead, Horiguchi is only concerned with how to display stored images. Thus, one skilled in the art would find nothing in the teachings of Horiguchi relevant to the design of an image processor. In other words, Horiguchi fails to provide any suggestion or motivation for somehow adapting its teachings for use in an image processor. Thus, not only does Horiguchi fail to teach storage of address information of image data while it is being processed, Horiguchi fails to provide any suggestion or motivation for doing so.

Therefore, it follows that if one skilled in the art were to consider the proposed combination of Hino and Horiguchi, this proposed combination would still fail to disclose or suggest "an address memory storing address information for each respective image data while being processed by said plurality of processors" as recited in claim 1. Since the proposed combination of Hino and Horiguchi fails to disclose or suggest all of the limitations of claim 1, the proposed combination of Hino and Horiguchi cannot render obvious claim 1, or claims 2-5 which depend from claim 1.

With respect to claim 6 (and claims 7-10, which depend from claim 6), this claim recites "memory storing arrangement information in original image data for said plurality of divided data." Thus, claim 6 is considered to patentably distinguish the proposed combination of Hino and Horiguchi for the reasons discussed in connection with claim 1.

With respect to claim 11, this claim as amended recites "dividing input image data" and "storing address information indicating arrangement of said divided image data." Claim 11 further recites "performing image processing on said divided image data with a plurality of processors." Thus, claim 11 has been amended to recite the storing of address information for image data along with processing the image data. Therefore, claim 11 as amended is considered to patentably distinguish the proposed combination of Hino and Horiguchi for the reasons discussed in connection with claim 1.

Accordingly, it is respectfully requested that the rejection of claims 1-11 under 35 U.S.C. § 103(a) over Hino in view of Horiguchi be reconsidered and withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, this application is considered to be in condition for allowance, and an early reconsideration and a Notice of Allowance are earnestly solicited.

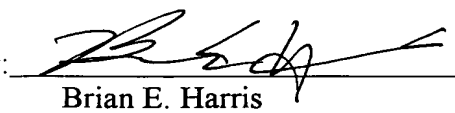
This Amendment does not increase the number of independent claims, does not increase the total number of claims, and does not present any multiple dependency claims. Accordingly, no fee based on the number or type of claims is currently due. However, if a fee, other than the issue fee, is due, please charge this fee to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260.

If an extension of time is required to enable this document to be timely filed and there is no separate Petition for Extension of Time filed herewith, this document is to be construed as also constituting a Petition for Extension of Time Under 37 C.F.R. §1.136(a) for a period of time sufficient to enable this document to be timely filed.

Any fee required for such Petition for Extension of Time, and any other fee required by this document, other than the issue fee, and not submitted herewith, should be

charged to Sidley Austin Brown & Wood LLP's Deposit Account No. 18-1260. Any refund should be credited to the same account.

Respectfully submitted,

By: 

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